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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,263	WANG ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10,12-14 and 26-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,12-14 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 10, 12-14, 26-30, and new claim 31 have been considered. New claim 31 has been added as per Applicant's request. Claims 1-9, 11, and 15-25 have been cancelled as per Applicant's request. Claims 10 and 26 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 05 June 2007 and Extension of Time for 3 Months as filed 05 June 2007.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10, 12-14, 26, 28, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar, U.S. Patent Number 5,506,976 (herein referred to as Jaggar) in view of Stiles et al., U.S. Number 5,515,518 (herein referred to as Stiles) in view of Yeh et al., U.S. Number 5,742,804 (herein referred to as Yeh) .

5. Referring to claim 10, Jaggar has taught a processor comprising:

a. A processor pipeline to output branch instruction addresses (Jaggar column 1, lines 64-67 and column 3, lines 49-51);

b. A branch target buffer responsive to the branch instruction addresses, wherein the branch target buffer comprises branch target buffer records to map branch

instruction addresses to branch target addresses (Jaggar column 2, lines 30-38 and column 6, lines 55-62);

c. A presbyopic target buffer responsive to the branch target buffer, wherein the presbyopic target buffer comprises presbyopic target buffer records to map branch target addresses to subsequent branch target addresses (Jaggar column 2, lines 30-38 and 40-48; column 3, lines 5-8; and column 6, lines 55-62);

d. A cache memory to retrieve the instructions at the branch target addresses and the instructions at the subsequent branch target addresses (Jaggar column 1, lines 64-67; column 3, lines 49-51; and column 6, lines 44-48); and

e. A fetch buffer to receive the instructions at the branch target addresses (Jaggar column 1, lines 64-67; column 3, lines 49-51; and column 6, lines 44-48).

6. Jaggar has not taught wherein the branch target buffer records comprise confidence counters to track a number of times branches associated with the branch target addresses are taken. Stiles has taught wherein the branch target buffer records comprise confidence counters to track a number of times branches associated with the branch target addresses are taken (Stiles column 2, lines 21-32). In regards to Stiles, the branch target buffer used some type of method or apparatus to track whether a branch would be taken or not, just as the confidence counter would track whether a branch is taken or not. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating a confidence counters reduces or eliminates the impact of branches on instruction flow (Stiles column 1, lines 57-58 and column 2, lines 9-11). Therefore, it would have been obvious to a person of ordinary skill in the art at the

time the invention was made to incorporate the prediction of Stiles in the branch target buffer of Jaggar to minimize the impact of branches on instruction flow.

7. In addition, Jaggar has not taught a prefetch stream buffer to receive the instructions at the subsequent branch target addresses. Yeh has taught a prefetch stream buffer to receive the instructions at the subsequent branch target addresses (Yeh column 1, lines 23-29 and column 2, lines 49-55). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating prefetch decreases the instruction fetch penalty (Yeh column 1, lines 39-44). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the prefetch of Yeh in the device of Jaggar to decrease the amount of time needed to fetch an instruction.

8. Referring to claim 12, Jaggar in view of Stiles in view of Yeh has taught the processor of claim 10 wherein the presbyopic target buffer is configured to be recursively searched to predict a plurality of subsequent branch target addresses (Yeh column 2, lines 49-50).

9. Referring to claim 13, Jaggar in view of Stiles in view of Yeh has taught the processor of claim 10 wherein the presbyopic target buffer implements skip-adjacent mapping (Jaggar column 2, lines 40-48).

10. Referring to claim 14, Jaggar in view of Stiles in view of Yeh has taught the processor of claim 10 wherein a complete branch target address is specified by a fixed number of bits, and the presbyopic target buffer includes mapping records that specify branch target addresses using less than the fixed number of bits (Jaggar column 2, lines 30-38 and 40-48; column 3, lines 5-8; and column 6, lines 55-62).

11. Referring to claim 26, Jaggar has taught a method comprising:

a. Processing instructions in a processor pipeline, wherein the processing is to output branch instruction addresses (Jaggar column 1, lines 64-67 and column 3, lines 49-51);

b. In a first buffer that maps branch instruction addresses to block entry addresses, searching for a first buffer record having a branch instruction address that matches a current instruction address (Jaggar column 2, lines 30-38 and column 6, lines 55-62); and

c. After the first buffer record is found, searching a second buffer that maps block entry addresses to subsequent block entry addresses for a second buffer record having a block entry address matching the first buffer record (Jaggar column 2, lines 30-38 and 40-48; column 3, lines 5-8; and column 6, lines 55-62).

12. Jaggar has not taught

a. After the first buffer record is found, incrementing a confidence counter in the first buffer record; and

b. After the second buffer record is found, incrementing a confidence counter in the second buffer record.

13. Stiles has taught

a. After the first buffer record is found, incrementing a confidence counter in the first buffer record (Stiles column 2, lines 21-32). In regards to Stiles, the branch target buffer used some type of method or apparatus to track whether a branch would be taken or not, just as the confidence counter would track whether a branch is taken or not.

b. After the second buffer record is found, incrementing a confidence counter in the second buffer record (Stiles column 2, lines 21-32). In regards to Stiles, the branch target buffer used some type of method or apparatus to track whether a branch would be taken or not, just as the confidence counter would track whether a branch is taken or not.

14. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating a confidence counters reduces or eliminates the impact of branches on instruction flow (Stiles column 1, lines 57-58 and column 2, lines 9-11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the prediction of Stiles in the branch target buffer of Jaggar to minimize the impact of branches on instruction flow.

15. In addition, Jaggar has not taught prefetching instructions beginning at a subsequent block entry address included in the second buffer record. Yeh has taught after the second buffer record is found, incrementing a confidence counter in the second buffer record and prefetching instructions beginning at a subsequent block entry address included in the second buffer record (Yeh column 1, lines 23-29 and column 2, lines 49-55). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating prefetch decreases the instruction fetch penalty (Yeh column 1, lines 39-44). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the prefetch of Yeh in the device of Jaggar to decrease the amount of time needed to fetch an instruction.

16. Referring to claim 28, Jaggar in view of Stiles in view of Yeh has taught the method of claim 26 further comprising:

a. Searching the second buffer recursively (Yeh column 2, lines 49-5); and

b. For each matching record found in the second buffer, each matching record having a corresponding subsequent block entry address, prefetching instructions from each of the corresponding subsequent block entry addresses (Yeh column 1, lines 23-29 and column 2, lines 49-55).

17. Referring to claims 30 and 31, Jaggar in view of Stiles in view of Yeh has taught

a. Wherein each recursive search represents a predicted branch, the method further comprising flushing from the stream buffer instructions prefetched as a result of a mispredicted branch (Applicant's claim 30) (Stiles column 16, lines 26-31). In regards to Stiles, in order to completely flush the pipeline, the buffer with the prefetched instructions must be flushed so that the next set of correct instructions may be prefetched and for the pipeline to be completely corrected.

b. Wherein the presbyopic target buffer records comprise confidence counters to track a number of times branches associated with the subsequent branch target addresses are taken (Applicant's claim 31) (Stiles column 2, lines 21-32). In regards to Stiles, the branch target buffer used some type of method or apparatus to track whether a branch would be taken or not, just as the confidence counter would track whether a branch is taken or not.

18. Claims 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Stiles in view of Yeh as applied to claims 26 and 28 above, and further in view of Papadopoulos, U.S. Patent Number 5,412,799 (herein referred to as Papadopoulos).

19. Referring to claims 27 and 29, Jaggar in view of Stiles in view of Yeh has taught

    a. Wherein prefetching comprises entering instructions into a stream buffer (Applicant's claim 27) (Yeh column 1, lines 23-29 and column 2, lines 49-55).

    b. Wherein prefetching comprises (Applicant's claim 27):

        i. Entering instructions into a stream buffer (Yeh column 1, lines 23-29 and column 2, lines 49-55).

20. Jaggar in view of Stiles in view of Yeh has not taught

    a. The stream buffer having a coloring field for each instruction entered (Applicant's claim 27).

    b. Wherein prefetching comprises (Applicant's claim 27):

        i. The stream buffer having a coloring field for each instruction entered; and

        ii. Assigning a different color to instructions fetched from different subsequent block entry addresses.

21. Papadopoulos has taught

    a. The stream buffer having a coloring field for each instruction entered (Applicant's claim 27) (Papadopoulos columns 10-11, lines 61-70).

    b. Wherein prefetching comprises (Applicant's claim 27):

        i. The stream buffer having a coloring field for each instruction entered (Papadopoulos columns 10-11, lines 61-70); and

        ii. Assigning a different color to instructions fetched from different subsequent block entry addresses (Papadopoulos columns 10-11, lines 61-70).

22. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating coloring fields benefits performance tuning and program analysis (Papadopoulos column 10, lines 60-61). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the coloring field of Papadopoulos in the device of Jaggar in view of Stiles in view of Yeh to improve performance tuning and program analysis.

Response to Arguments

23. Applicant's arguments with respect to claims 10, 12-14, 26-30, and new claim 31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Examiner
Art Unit 2183

19 August 2007

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